CLAIMS

1. A logic circuit for generation of a carry bit output by combining two sets of binary inputs, the logic circuit comprising first logic for receiving a plurality of bits of the binary inputs and for generating at least one intermediate output; final logic for receiving at least one intermediate output of the first logic and for generating the carry bit output; wherein said final logic is arranged to generate the carry bit output using a reduced generate function for a group of bits of the binary inputs and at least one intermediate output from said first logic at least one of which is generated as a reduced generate function of a sub-group of bits of the binary inputs; wherein a reduced generate function for a group of bits, partitioned into at least one most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; and wherein first logic and/or said final logic is arranged to use a reduced generate function in which the group or sub-group of bits of the binary inputs is partitioned so that said at least one most significant bit comprises at least two most significant bits.

2. A logic circuit for generation of a sum bit output by combining two sets of binary inputs, the logic circuit comprising first logic for receiving a plurality of bits of the binary inputs and for generating at least one intermediate output; final logic for receiving at least one intermediate output of the first logic and for generating the sum bit output; wherein said final logic is arranged to generate the sum bit output using a reduced generate function for a group of bits of the binary inputs and at least one intermediate output from said first logic at least one of which is generated as a reduced generate function of a sub-group of bits of the binary inputs; wherein a reduced generate function for a group of bits, partitioned into at least one most significant bit and at least

one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; and wherein first logic and/or said final logic is arranged to use a reduced generate function in which the group or sub- group of bits of the binary inputs is partitioned so that said at least one most significant bit comprises at least two most significant bits.

3. A logic circuit according to claim 1 or claim 2, wherein the final logic includes at least one multiplexer.

4. A logic circuit for generation of a carry bit output by combining two sets of binary inputs, the logic circuit comprising a first level of logic comprising a plurality of logic units, each logic unit for receiving a plurality of bits of the binary inputs and for generating an intermediate output; at least one further level of logic including a final level of logic for receiving at least one intermediate output of at least one previous level of logic and comprising at least one logic unit for receiving at least one intermediate output from at least one logic unit of at least one previous level and for generating an intermediate output; and output logic for generating the carry bit output using at least one intermediate output from the final level of logic; wherein at least one logic unit of at least one level of logic is arranged to generate an intermediate output as a reduced generate function for a group of bits of the binary inputs using at least one intermediate output from at least one higher level at least one of which is generated as a reduced generate function of a sub-group of bits of the binary inputs; wherein an intermediate output generated as a reduced generate function for a group or sub-group of bits, partitioned into at least one most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out

of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; and wherein at least one of said at least one logic unit of at least one level of logic is arranged to generate an intermediate output as a reduced generate function in which the group or sub-group of bits of the binary inputs for said at least one logic unit is partitioned so that said at least one most significant bit comprises at least two most significant bits.

5. A logic circuit according to claim 4, including further logic for generating an output for a group of most significant bits of the binary inputs which is high if a carry is generated out of the group or if all of the bit level propagate bits for the group are high, wherein said output logic is arranged to generate the carry bit as a function of the logical AND of the output of said further logic and at least one intermediate output of said final level generated as a reduced generate function for a group of bits.

6. A logic circuit for generation of a sum bit output by combining two sets of binary inputs, the logic circuit comprising a first level of logic comprising a plurality of logic units, each logic unit for receiving a plurality of bits of the binary inputs and for generating an intermediate output; at least one further level of logic including a final level of logic for receiving outputs of at least one previous level of logic and comprising at least one logic unit for receiving at least one intermediate output from at least one logic unit of at least one previous level and for generating an intermediate output; and output logic for generating the sum bit output using at least at least one intermediate output from the final level of logic; wherein at least one logic unit of at least one level of logic is arranged to generate an intermediate output as a reduced generate function for a group of bits of the binary inputs using at least one intermediate output from at least one higher level at least one of which is generated as a reduced generate function of a sub-group of bits of the binary inputs; wherein an intermediate output generated as a reduced generate function for a group or sub-group of bits, partitioned into at least one

most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; and wherein at least one of said at least one logic unit of at least one level of logic is arranged to generate an intermediate output as a reduced generate function in which the group or sub-group of bits of the binary inputs for said at least one logic unit is partitioned so that said at least one most significant bit comprises at least two most significant bits.

7. A logic circuit according to claim 6, wherein the output logic comprises a multiplexer.

8. A logic circuit according to claim 6 or claim 7, including further logic for generating an output for a group of most significant bits of the binary inputs which is high if a carry is generated out of the group or if all of the bit level propagate bits for the group are high, wherein said output logic is arranged to generate the carry bit as a function of the logical AND of the output of said further logic and at least one intermediate output of said final level generated as a reduced generate function for a group of bits.

9. A logic circuit for generation of a carry bit output by combining two sets of binary inputs, the logic circuit comprising a first level of logic comprising a plurality of logic units, each logic unit for receiving a plurality of bits of the binary inputs and for generating an intermediate output; at least one further level of logic for receiving outputs of at least one previous level of logic and comprising at least one logic unit for receiving the intermediate outputs from at least one logic unit of the at least one previous level and for generating an intermediate output; a final level of logic for receiving outputs of at least one previous level of logic and comprising at least one logic

unit for receiving at least one intermediate output from at least one logic unit of the at least one previous level of logic and for generating the carry bit output; wherein at least one logic unit of at least one of said further levels of logic is arranged to generate an intermediate output as a reduced generate function for a group of bits of the binary inputs using at least one intermediate output from at least one higher level, at least one of said intermediate outputs being generated as a reduced generate function of a sub-group of bits of the binary inputs; wherein an intermediate output generated as a reduced generate function for a group or sub-group of bits, partitioned into at least one most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; and wherein at least one of said at least one logic unit of at least one of said first or further levels of logic is arranged to generate an intermediate output as a reduced generate function in which the group or sub-group of bits of the binary inputs for said at least one logic unit is partitioned so that said at least one most significant bit comprises at least two most significant bits.

10. A logic circuit for generation of a sum bit output by combining two sets of binary inputs, the logic circuit comprising a first level of logic comprising a plurality of logic units, each logic unit for receiving a plurality of bits of the binary inputs and for generating an intermediate output; at least one further level of logic for receiving at least one intermediate output of at least one previous level of logic and comprising at least one logic unit for receiving at least one intermediate output from at least one logic unit of the at least one previous level and for generating an intermediate output; a final level of logic for receiving at least one intermediate output of at least one previous level of logic and comprising at least one logic unit for receiving at least one intermediate output from at least one logic unit of the at least one previous level of logic and for

generating the sum bit output; wherein at least one logic unit of at least one of said further levels of logic is arranged to generate an intermediate output as a reduced generate function for a group of bits of the binary inputs using intermediate outputs from at least one higher level, at least one of said intermediate outputs being generated as a reduced generate function of a sub-group of bits of the binary inputs; wherein an intermediate output generated as a reduced generate function for a group or sub-group of bits, partitioned into at least one most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; and wherein at least one of said at least one logic unit of at least one of said first or further levels of logic is arranged to generate an intermediate output as a reduced generate function in which the group or sub-group of bits of the binary inputs for said at least one logic unit is partitioned so that said at least one most significant bit comprises at least two most significant bits.

11. A logic circuit according to claim 10, wherein the final level of logic includes at least one multiplexer.

12. A logic circuit for generation of a carry bit output by combining two sets of binary inputs, the logic circuit comprising first logic comprising a plurality of logic units, each logic unit for receiving a plurality of bits of the binary inputs and for generating an intermediate output; final logic for receiving at least one intermediate output of the first logic and comprising at least one logic unit for receiving at least one intermediate output from at least one logic unit of the first logic and for generating the carry bit output; wherein at least one logic unit of at least one of said first logic is arranged to generate an intermediate output as a reduced generate function for a group of bits of the binary inputs; wherein an intermediate output generated as a reduced

generate function for a group of bits, partitioned into at least one most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; and wherein at least one of said at least one logic unit of said first logic is arranged to generate an intermediate output for receipt by said final logic as a reduced generate function in which the group of bits of the binary inputs for said at least one logic unit is partitioned so that said at least one most significant bit comprises at least two most significant bits.

13. A logic circuit for generation of a sum bit output by combining two sets of binary inputs, the logic circuit comprising first logic comprising a plurality of logic units, each logic unit for receiving a plurality of bits of the binary inputs and for generating an intermediate output; final logic for receiving at least one intermediate output of the first logic and comprising at least one logic unit for receiving at least one intermediate output from at least one logic unit of the first logic and for generating the sum bit output; wherein at least one logic unit of at least one of said first logic is arranged to generate an intermediate output as a reduced generate function for a group of bits of the binary inputs; wherein an intermediate output generated as a reduced generate function for a group of bits, partitioned into at least one most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; and wherein at least one of said at least one logic unit of said first logic is arranged to generate an intermediate output for

receipt by said final logic as a reduced generate function in which the group of bits of the binary inputs for said at least one logic unit is partitioned so that said at least one most significant bit comprises at least two most significant bits.

14. A logic circuit according to claim 13, wherein the final logic includes at least one multiplexer.

15. A logic circuit for generation of a carry bit output by combining two sets of binary inputs, the logic circuit comprising: bit level carry generate and propagate function logic for receiving the binary inputs and for generating bit level carry generate and propagate function bits for said binary inputs by respectively logically AND and OR combining respective bits of said binary inputs; first logic for receiving bit level carry generate and propagate function bits for a first group of at least three most significant bits of said binary inputs to generate a high output if a carry is generated out of the first group of most significant bits of said binary input or if said carry propagate function bits for the most significant bits are all high; second logic for receiving bit level carry generate and propagate function bits for said binary inputs to generate a high output if any of said carry generate function bits for the most significant bits are high or if a carry is generated out of a second group of least significant bits of said binary input; and combining logic for generating the carry bit output by combining outputs of said first and second logic.

16. A logic circuit for generation of a sum bit output by combining two sets of binary inputs, the logic circuit comprising: bit level carry generate and propagate function logic for receiving the binary inputs and for generating bit level carry generate and propagate function bits for said binary inputs by respectively logically AND and OR combining respective bits of said binary inputs; first logic for receiving bit level carry generate and propagate function bits for a first group of at least three most significant bits of said binary inputs to generate a high output if a carry is generated out of the first group of most significant bits of said binary input or if said carry propagate function bits for the most significant bits are all high; second logic for receiving bit

level carry generate and propagate function bits for said binary inputs to generate a high output if any of said carry generate function bits for the most significant bits are high or if a carry is generated out of a second group of least significant bits of said binary input; and combining logic for generating the sum bit output by combining outputs of said first and second logic.

17. A logic circuit according to claim 16, wherein the combining logic includes at least one multiplexer.

18. A logic circuit according to claim 16 or claim 17, wherein the first logic comprises a plurality of first logic modules each for receiving bit level carry generate and propagate function bits for subgroups of the first group of at least three most significant bits of the binary inputs to generate a high output if a carry is generated for the subgroup of most significant bits of the binary input or if the carry propagate function bits for the subgroup of most significant bits are all high.

19. A logic circuit according to any one of claims 16 to 17, wherein the second logic comprises a plurality of logic modules for receiving subgroups of the second group of least significant bits of the binary input to generate a carry for each of the subgroups and combining logic for combining the generated carrys.

20. A logic circuit for generation of a carry bit output by combining two sets of binary inputs, the logic circuit comprising: bit level carry generate and propagate function logic for receiving the binary inputs and for generating bit level carry generate and propagate function bits for said binary inputs by respectively logically AND and OR combining respective bits of said binary inputs; first logic for receiving bit level generate and propagate function bits for a first group of at least three most significant bits of said binary inputs to generate an output as a function of a logical OR combination of a carry bit output for the first group of most significant bits of said binary input and a result of a logical AND combination of propagate function bits for the most significant bits; second logic for receiving bit level generate and propagate

function bits for said binary inputs to generate an output as a function of a result of a logical OR combination of a carry bit output for a group of least significant bits of said binary inputs and a function B which is high if a carry is generated at any bit position in the most significant bits; and combining logic for generating the carry bit output by combining outputs of said first and second logic.

21. A logic circuit for generation of a sum bit output by combining two sets of binary inputs, the logic circuit comprising: bit level carry generate and propagate function logic for receiving the binary inputs and for generating bit level carry generate and propagate function bits for said binary inputs by respectively logically AND and OR combining respective bits of said binary inputs; first logic for receiving bit level generate and propagate function bits for a first group of at least three most significant bits of said binary inputs to generate an output as a function of a logical OR combination of a carry bit output for the first group of most significant bits of said binary input and a result of a logical AND combination of propagate function bits for the most significant bits; second logic for receiving bit level generate and propagate function bits for said binary inputs to generate an output as a function of a result of a logical OR combination of a carry bit output for a group of least significant bits of said binary inputs and a function B which is high if a carry is generated at any bit position in the most significant bits; and combining logic for generating the sum bit output by combining outputs of said first and second logic.

22. A logic circuit according to claim 21, wherein the combining logic includes at least one multiplexer.

23. A binary adder circuit comprising the logic circuit according to any one of claims 1, 4, 5, 9, 12, 15, or 20, including addition logic comprising exclusive OR logic and a multiplexer for determining an addition result including said carry bit for said binary inputs.

24. A comparison logic circuit for comparing two binary inputs comprising the logic circuit according to any one of claims 1, 4, 5, 9, 12, 15,or 20, including logic for using said carry bit to indicate whether one binary input represents a binary number less than or more than another binary number represented by the other binary input.

25. A logic circuit for generation of a carry or sum bit output by adding two sets of binary inputs plus one, the logic circuit comprising first logic for receiving a plurality of bits of the binary inputs and for generating at least one intermediate output; final logic for receiving at least one intermediate output of the first logic and for generating the carry or sum bit output; wherein said final logic is arranged to generate the carry or sum bit output using a reduced modified generate function for a group of bits of the binary inputs and at least one intermediate output from said first logic at least one of which is generated as a reduced generate function or a reduced modified generate function of a sub-group of bits of the binary inputs; wherein a reduced generate function for a group of bits, partitioned into at least one most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; wherein a reduced modified generate function is the logical OR of a modified generate function for the least significant bits and the function X for the most significant bits, where the modified generate function is high if a carry is generated on adding the least significant bits plus one and low if not; wherein said final logic is arranged to use a reduced modified generate function in which the group or sub-group of bits of the binary inputs is partitioned so that said at least one most significant bit comprises at least two most significant bits and/or said first logic is arranged to use a reduced generate function or a reduced modified generate function in which the group or sub-group of bits of the binary inputs is partitioned so that said at least one most significant bit comprises at least two most significant bits.

26. A logic circuit according to claim 25, wherein said reduced modified generate function uses a hyper propagate function for the group of bits, the hyper propagate function comprises a logical AND combination of the modified generate function for at least one least significant bit of the group of bits and a propagate function for at least one most significant bit of the group of bits, and the propagate function is high if a carry into a group of bits would be propagated out of the group of bits.

27. A logic circuit according to claim 26, wherein a hyper propagate function for a group of bits uses a hyper propagate function for a sub-group of bits.

28. A logic circuit for generation of a carry or sum bit output by adding two sets of binary inputs plus one, the logic circuit comprising a first level of logic comprising a plurality of logic units, each logic unit for receiving a plurality of bits of the binary inputs and for generating an intermediate output; at least one further level of logic including a final level of logic for receiving at least one intermediate output of at least one previous level of logic and comprising at least one logic unit for receiving at least one intermediate output from at least one logic unit of at least one previous level and for generating an intermediate output; and output logic for generating the carry or sum bit output using at least one intermediate output from the final level of logic; wherein at least one logic unit of at least one level of logic is arranged to generate an intermediate output as a reduced generate function or a for a reduced modified generate function group of bits of the binary inputs using at least one intermediate output from at least one higher level at least one of which is generated as a reduced generate function or reduced modified generate function group of a sub-group of bits of the binary inputs; wherein an intermediate output generated as a reduced generate function for a group or sub-group of bits, partitioned into at least one most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit

position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; wherein a reduced modified generate function is the logical OR of a modified generate function for the least significant bits and the function X for the most significant bits, where the modified generate function is high if a carry is generated on adding the least significant bits plus one and low if not; and wherein at least one of said at least one logic unit of at least one level of logic is arranged to generate an intermediate output as a reduced generate function or reduced modified generate function in which the group or sub-group of bits of the binary inputs for said at least one logic unit is partitioned so that said at least one most significant bit comprises at least two most significant bits.

29. A logic circuit according to claim 28, wherein said reduced modified generate function uses a hyper propagate function for the group of bits, the hyper propagate function comprises a logical AND combination of the modified generate function for at least one least significant bit of the group of bits and a propagate function for at least one most significant bit of the group of bits, and the propagate function is high if a carry into a group of bits would be propagated out of the group of bits.

30. A logic circuit according to claim 29, wherein a hyper propagate function for a group of bits uses a hyper propagate function for a sub-group of bits.

31. A logic circuit according to claim 30, including further logic for generating an output for a group of most significant bits of the binary inputs which is high if a carry is generated out of the group or if all of the bit level propagate bits for the group are high, wherein said output logic is arranged to generate the carry bit as a function of the logical AND of the output of said further logic and the intermediate output of said final level generated as a reduced modified generate function for a group of bits.

32. A logic circuit for generation of a carry or sum bit output by adding two sets of binary inputs plus one, the logic circuit comprising a first level of logic comprising a

plurality of logic units, each logic unit for receiving a plurality of bits of the binary inputs and for generating an intermediate output; at least one further level of logic for receiving at least one intermediate output of at least one previous level of logic and comprising at least one logic unit for receiving at least one intermediate output from at least one logic unit of the at least one previous level and for generating an intermediate output; a final level of logic for receiving at least one intermediate output of at least one previous level of logic and comprising at least one logic unit for receiving at least one intermediate output from at least one logic unit of the at least one previous level of logic and for generating the carry or sum bit output; wherein at least one logic unit of at least one of said further levels of logic is arranged to generate an intermediate output as a reduced generate function or a reduced modified generate function for a group of bits of the binary inputs using at least one intermediate output from at least one higher level, at least one of said intermediate outputs being generated as a reduced generate function or a reduced modified generate function of a sub-group of bits of the binary inputs; wherein an intermediate output generated as a reduced generate function for a group or sub-group of bits, partitioned into at least one most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; wherein a reduced modified generate function is the logical OR of a modified generate function for the least significant bits and the function X for the most significant bits, where the modified generate function is high if a carry is generated on adding the least significant bits plus one and low if not; and wherein at least one of said at least one logic unit of at least one of said first or further levels of logic is arranged to generate an intermediate output as a reduced generate function or reduced modified generate function in which the group or sub-group of bits of the binary inputs for said at least one logic unit is partitioned so that said at least one most significant bit comprises at least two most significant bits.

33. A logic circuit according to claim 32, wherein said reduced modified generate function uses a hyper propagate function for the group of bits, the hyper propagate function comprises a logical AND combination of the modified generate function for at least one least significant bit of the group of bits and a propagate function for at least one most significant bit of the group of bits, and the propagate function is high if a carry into a group of bits would be propagated out of the group of bits.

34. A logic circuit according to claim 33, wherein a hyper propagate function for a group of bits uses a hyper propagate function for a sub-group of bits.

35. A logic circuit for generation of a carry or sum bit output by adding two sets of binary inputs plus one, the logic circuit comprising first logic comprising a plurality of logic units, each logic unit for receiving a plurality of bits of the binary inputs and for generating an intermediate output; final logic for receiving at least one intermediate output of the first logic and comprising at least one logic unit for receiving at least one intermediate output from at least one logic unit of the first logic and for generating the carry or sum bit output; wherein at least one logic unit of at least one of said first logic is arranged to generate an intermediate output as a reduced generate function or a reduced modified generate function for a group of bits of the binary inputs; wherein an intermediate output generated as a reduced generate function for a group of bits, partitioned into at least one most significant bit and at least one least significant bit, is the logical OR of a generate function for the least significant bits and a function X for the most significant bits, where the generate function is high if a carry is generated out of the least significant bits and low if not, and X is a function which is high if a carry is generated out of the most significant bits, low if no carry is generated at any bit position in the most significant bits, and in a don't care state if a carry is generated at some bit position in the most significant bits but no carry is generated out of the most significant bits; wherein a reduced modified generate function is the logical OR of a modified generate function for the least significant bits and the function X for the most significant bits, where the modified generate function is high if a carry is generated on adding the

least significant bits plus one and low if not; and wherein at least one of said at least one logic unit of said first logic is arranged to generate an intermediate output for receipt by said final logic as a reduced generate function or a reduced modified generate function in which the group of bits of the binary inputs for said at least one logic unit is partitioned so that said at least one most significant bit comprises at least two most significant bits.

36. A logic circuit according to claim 35, wherein said reduced modified generate function uses a hyper propagate function for the group of bits, the hyper propagate function comprises a logical AND combination of the modified generate function for at least one least significant bit of the group of bits and a propagate function for at least one most significant bit of the group of bits, and the propagate function is high if a carry into a group of bits would be propagated out of the group of bits.

37. A logic circuit according to claim 36, wherein a hyper propagate function for a group of bits uses a hyper propagate function for a sub-group of bits.

38. A logic circuit for generation of a carry or sum bit output by adding two sets of binary inputs plus one, the logic circuit comprising: bit level carry generate and propagate function logic for receiving the binary inputs and for generating bit level carry generate and propagate function bits for said binary inputs by respectively logically AND and OR combining respective bits of said binary inputs; first logic for receiving bit level carry generate and propagate function bits for a first group of at least three most significant bits of said binary inputs to generate a high output if a carry is generated out of the first group of most significant bits of said binary input or if said carry propagate function bits for the most significant bits are all high; second logic for receiving bit level carry generate and propagate function bits for said binary inputs to generate a high output if any of said carry generate function bits for the most significant bits are high or if a carry is generated out of a second group of least significant bits plus one of said binary input; and combining logic for generating the carry or sum bit output by combining outputs of said first and second logic.

39. A logic circuit according to claim 38, wherein the first logic comprises a plurality of first logic modules, each for receiving bit level carry generate and propagate function bits for subgroups of the first group of at least three most significant bits of the binary inputs to generate a high output if a carry is generated for the subgroup of most significant bits of the binary input or if the carry propagate function bits for the subgroup of most significant bits are all high.

40. A logic circuit according to claim 38 or claim 39, wherein the second logic comprises a plurality of logic modules for receiving subgroups of the second group of least significant bits of the binary input to generate a carry for each of the subgroups and combining logic for combining the generated carrys.

41. A logic circuit for generation of a carry or sum bit output by adding two sets of binary inputs plus one, the logic circuit comprising: bit level carry generate and propagate function logic for receiving the binary inputs and for generating bit level carry generate and propagate function bits for said binary inputs by respectively logically AND and OR combining respective bits of said binary inputs; first logic for receiving bit level generate and propagate function bits for a first group of at least three most significant bits of said binary inputs to generate an output as a function of a logical OR combination of a carry bit output for the first group of most significant bits of said binary input and a result of a logical AND combination of propagate function bits for the most significant bits; second logic for receiving bit level generate and propagate function bits for said binary inputs to generate an output as a function of a result of a logical OR combination of a carry bit output for a group of least significant bits plus one of said binary inputs and a function B which is high if a carry is generated at any bit position in the most significant bits; and combining logic for generating the carry or sum bit output by combining outputs of said first and second logic.

42. A logic circuit for generation of a carry bit output by combining two sets of binary inputs, the logic circuit comprising logic for receiving a plurality of bits of the

binary inputs and for generating the carry bit output; wherein said logic is arranged to generate the carry bit output as the logical AND of a generate function for at least one most significant bit, a reduced modified generate function for the said at least one most significant bit and at least one middle bit of the binary inputs and a reduced generate function for said at least one middle bit and at least one least significant bit of the binary inputs; wherein said reduced generate function is the logical OR of a generate function for the at least one least significant bit and a function X for the at least one most significant bit and the at least one middle bit, where the generate function for the at least one least significant bit is high if a carry is generated out of the at least one least significant bit and low if not, and X is a function which is high if a carry is generated out of the at least one most significant bit and said at least one middle bit, low if no carry is generated at any bit position in the at least one most significant bit and said at least one middle bit, and in a don't care state if a carry is generated at some bit position in the at least one most significant bit and said at least one middle bit but no carry is generated out of the at least one most significant bit and said at least one middle bit; said reduced modified generate function is the logical OR of a modified generate function for the at least one middle bit and the function X for the most significant bits, where the modified generate function for the at least one middle bit is high if a carry is generated on adding the at least one middle bit plus one and low if not.

43. A logic circuit for generation of a carry bit output by combining two sets of binary inputs plus 1, the logic circuit comprising logic for receiving a plurality of bits of the binary inputs and for generating the carry bit output; wherein said logic is arranged to generate the carry bit output as the logical AND of a modified generate function for at least one most significant bit, a first reduced modified generate function for the said at least one most significant bit and at least one middle bit of the binary inputs and a second reduced modified generate function for said at least one middle bit and at least one least significant bit of the binary inputs; wherein said second reduced modified generate function is the logical OR of a modified generate function for the at least one least significant bit and a function X for the at least one most significant bit and the at least one middle bit, where the modified generate function for the at least one least

significant bit is high if a carry is generated out of the at least one least significant bit plus one and low if not, and X is a function which is high if a carry is generated out of the at least one most significant bit and said at least one middle bit, low if no carry is generated at any bit position in the at least one most significant bit and said at least one middle bit, and in a don't care state if a carry is generated at some bit position in the at least one most significant bit and said at least one middle bit but no carry is generated out of the at least one most significant bit and said at least one middle bit; said first reduced modified generate function is the logical OR of a modified generate function for the at least one middle bit and the function X for the most significant bits, where the modified generate function for the at least one middle bit is high if a carry is generated on adding the at least one middle bit plus one and low if not.

44. A method of designing a logic circuit for generating a carry or sum bit from the combination of two j-bit binary inputs, the method comprising:

performing a first parallelisation of the function $G_{j-1:0}$ for generating the carry in accordance with a first relationship $G_{a:c} = D_{a:b}(X_{a:b} + G_{b-1:c})$ to generate a parallelised function $D_{j-1:k}(X_{j-1:k} + G_{k-1:0})$, where G represents a generate function for a group of bits from j-1 to 0 or from k-1 to 0, D represents a logical OR of a generate function and a propagate function for a group of bits from j-1 to k, and X represents a function which is high if a carry is generated out of the j-1 to k bits, low if no carry is generated at any bit position in the j-1 to k bits, and in a don't care state if a carry is generated at some bit position in the j-1 to k bits but no carry is generated out of the j-1 to k bits;

performing a second parallelisation of the generate function of the parallelised function using a parallel prefix method to generate a further parallelised function; and

designing a logic circuit in accordance with the further parallelised function.

45. A method according to claim 44, including performing a further parallelisation of the further parallelised function using the first relationship to parallelise the generate function for a group of least significant bits.

46. A method according to claim 45, including performing a further parallelisation of the further parallelised function using a parallel prefix method to parallelise the further parallelised generate function for a group of least significant bits.

47. A method according to claim 44, including repeatedly performing further parallelisations of the further parallelised function using alternately the first relationship and a parallel prefix method to parallelise the generate function for a group of least significant bits.

48. A method according to any one of claims 44 to 47, including performing a parallelisation of D using a third relationship $D_{a:c} = D_{a:b} (X_{a:b} + D_{b-1:c})$ to generate a further parallelised function for use in the logic design.

49. A method according to claim 48, including performing a further parallelisation of D in the further parallelised function using a parallel prefix method.

50. A method according to claim 48, including repeatedly performing further parallelisations of D in the further parallelised function using alternately the third relationship and a parallel prefix method to parallelise D.

51. A method of building a logic circuit comprising the method of any one of claims 44 to 50, including building a logic circuit in accordance with the design.

52. A method according to claim 49, including repeatedly performing further parallelisations of D in the further parallelised function using alternately the third relationship and a parallel prefix method to parallelise D.

53. A logic circuit according to claim 18, wherein the second logic comprises a plurality of logic modules for receiving subgroups of the second group of least significant bits of the binary input to generate a carry for each of the subgroups and combining logic for combining the generated carrys.